Training LLMs with MXFP4

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Low Precision Training

Modern AI accelerators come with hardware acceleration for low precision (LP) matrix multiplications (GEMMs). Reducing the precision linearly increase GEMM throughput, making LP GEMMs attractive for compute-bound model training. However, reducing precision increases distortion, which can harm model quality.

Datatype	Scale Bits	Block Size	Exponent Bits	Mantissa Bits	Speedup vs. FP32
MXFP4	8	32	2	1	8X
FP8 E4M3	-	-	4	3	4X
FP8 E5M2	_	-	5	2	4X
FP16	-	-	5	10	2X
BF16	-	-	8	7	2X

One way to use LP GEMMs is with **mixed precision (MP) training**, which quantizes high precision parameters for LP GEMMs but performs updates in high precision. MP works for BF/FP16 and FP8, but is **insufficient for MXFP4**.

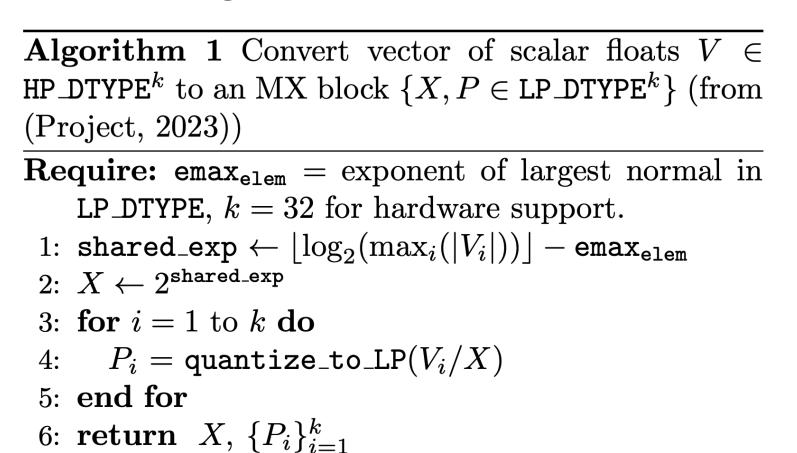
MXFP4

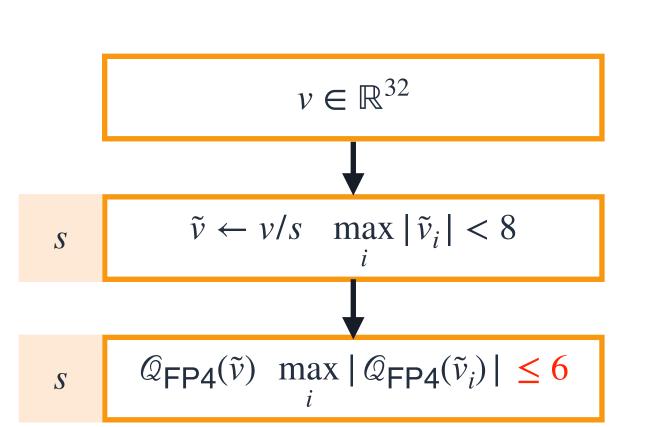
The MXFP4 datatype shares an INT8 scale across 32 contiguous FP4 entries in memory. The value represented by a scale s and block b is 2^sb

Shared INT8 Scale s

32 Contiguous FP4 Numbers

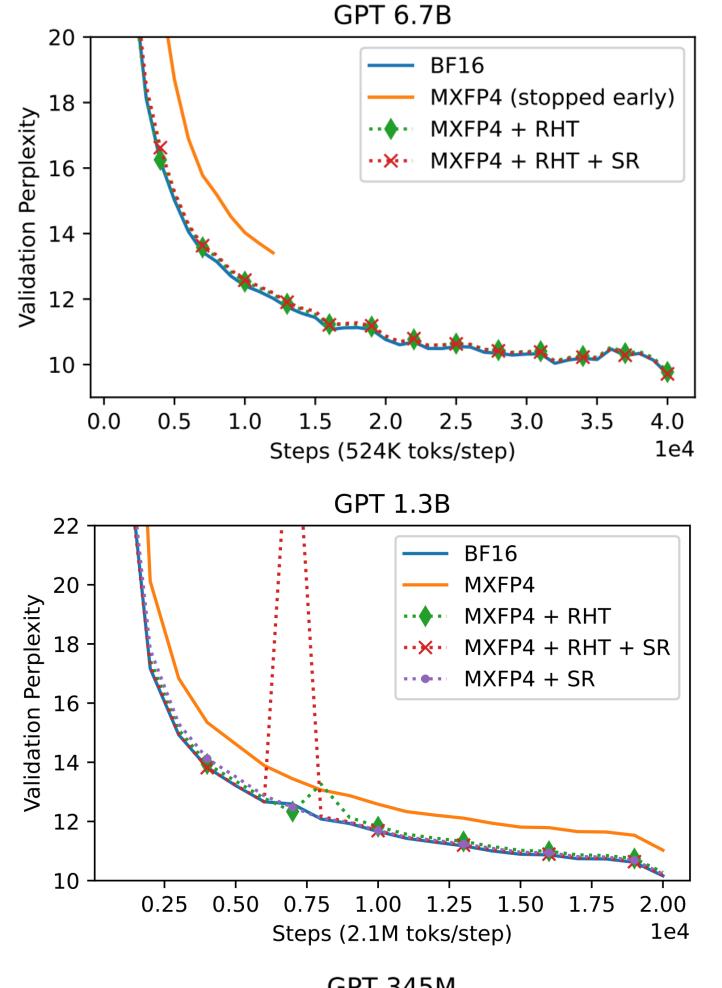
We can quantize a vector of reals to a MXFP4 vector in a hardware-efficient way with the OCP quantization algorithm (Algorithm 1). However, Algorithm 1 is **biased** since it scales elements to be < 8 (emax_{FP4} = 2) before quantizing to FP4. Since the largest FP4 value is 6, numbers between 6 and 8 get clipped to 6.





Pretraining & Finetuning Experiments

To test our recipe, we pretrained GPT 345M, 1.3B, and 6.7B models on up to 210B tokens of the Wikipedia corpus. Our recipe achieves a < **0.1 perplexity gap** vs. a BF16 backward pass and works with both BF16 and FP8 forward passes.



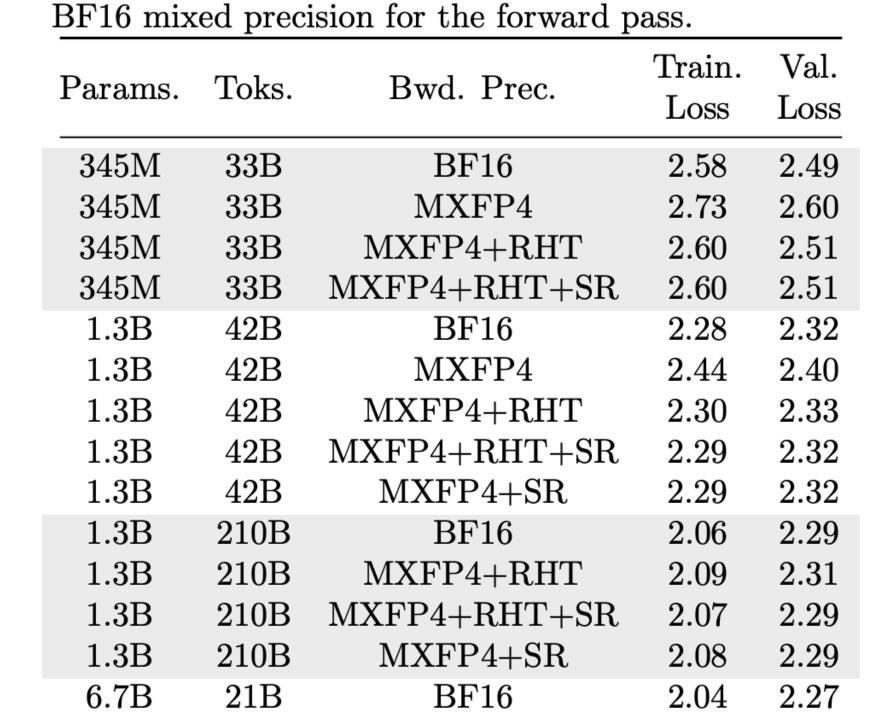
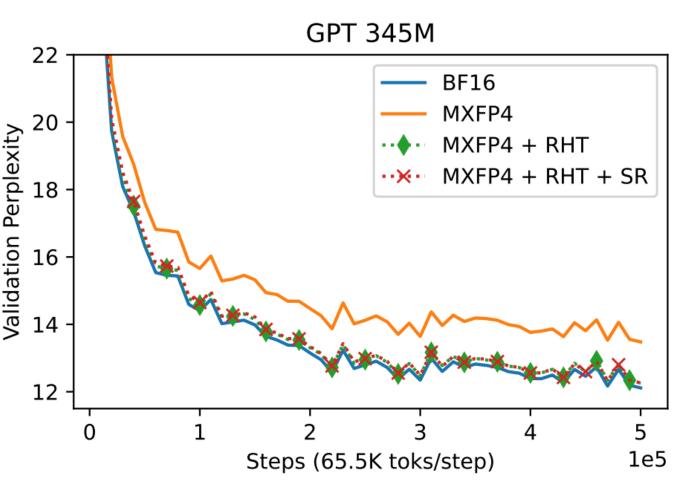


Table 2: Final losses for GPT models trained on the

GPT2 Wikipedia corpus. All models were trained with

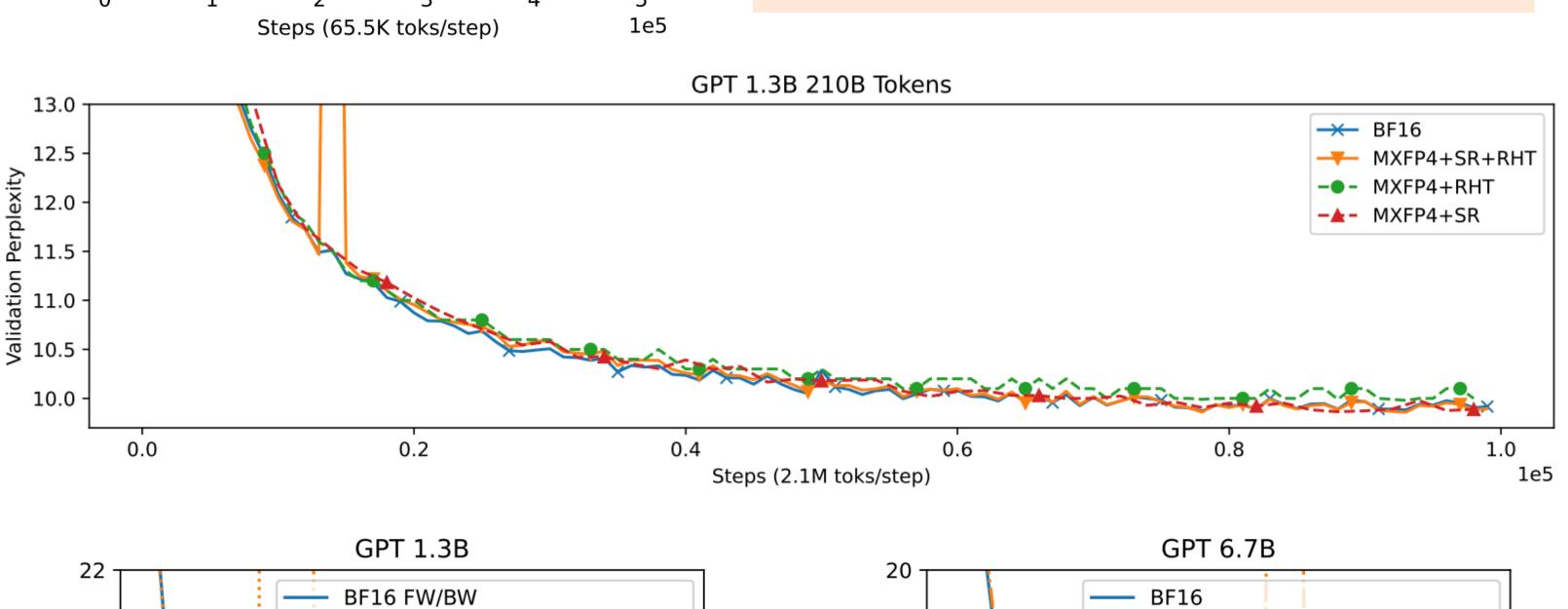


Downstream Finetuning Performance						
Model	ArcC	ArcE	PiQA	BoolQ	Wino	
BF16	23.1	49.2	60.5	53.3	52.0	
MXFP4	22.2	47.8	61.3	59.6	49.6	
BF16 Tulu2	25.6	50.6	62.7	59.6	51.6	
MXFP4 Tulu2	25.9	49.9	62.9	60.5	51.8	

MXFP4+RHT

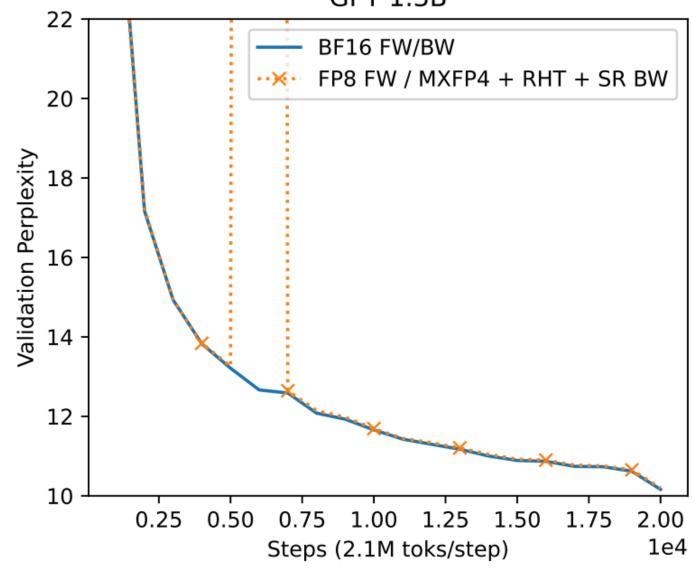
MXFP4+RHT+SR

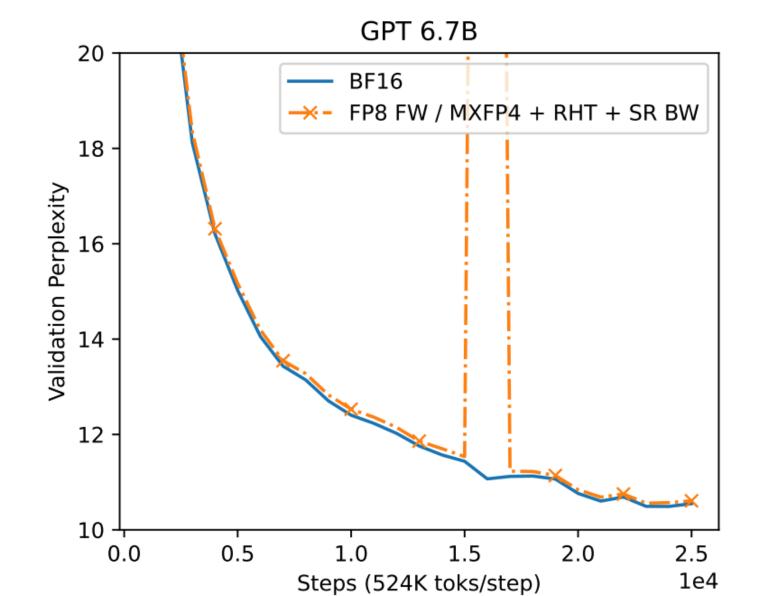
2.08



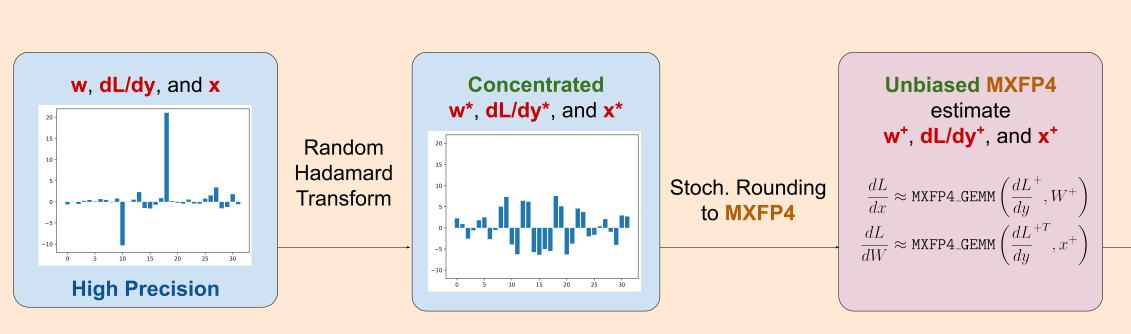
6.7B

6.7B





Our Approach



We present the first near-lossless MXFP4 training recipe using fully hardware-accelerated operations. We use MXFP4 to calculate unbiased gradient estimates for linear layers, which consists of >1/2 training FLOPs. Specifically,

Low Variance,

Unbiased gradients

computed in MXFP4

- We use stochastic rounding (SR) to make MX quantization unbiased.
- We use a memory-bound construction of the random Hadamard transform (RHT) to theoretically bound the variance of SR in gradient estimates.

Low Variance Unbiased Quantization

To achieve unbiased MXFP4 quantization, we use stochastic rounding (SR). The latest Al accelerators come with hardware SR support, making SR practical. In SR, inputs are randomly quantized such that the quantized number equals the original number *in expectation*. SR is usually implemented with *dithering*, which adds uniform random noise to an input before performing nearest rounding.

Algorithm 2 Unbiased quantization of
$$V \in HP_DTYPE^k$$
 to an MXFP4 block $\{X, P \in LP_DTYPE^k\}$ Require: $emax_{elem} = exponent$ of the largest normal number in LP_DTYPE $\delta \sim \mathcal{U}(-0.5, 0.5)$ 1: $shared_exp \leftarrow \lfloor log_2(max_i(|V_i|)) \rfloor - emax_{elem}$ $\delta \sim \mathcal{U}(-0.5, 0.5)$ 2: $X \leftarrow 2^{shared_exp}$ $SR_{dither}(x) = \begin{cases} \lfloor x \rfloor & x + \delta < \lfloor x \rfloor + \frac{1}{2} \\ \lceil x \rceil & x + \delta \geq \lfloor x \rfloor + \frac{1}{2} \end{cases}$ 3: $for i = 1 to k do$ $SR_{dither}(x) = \begin{cases} \lfloor x \rfloor & x + \delta < \lfloor x \rfloor + \frac{1}{2} \\ \lceil x \rceil & x + \delta \geq \lfloor x \rfloor + \frac{1}{2} \end{cases}$ 5: $P_i = stochastic_round_to_FP4(V_i/X)$ $SR_{dither}(x) = \begin{cases} log_1 & x + \delta \leq \lfloor x \rfloor + \frac{1}{2} \\ \lceil x \rceil & x + \delta \leq \lfloor x \rfloor + \frac{1}{2} \end{cases}$ 6: end for $SR_{dither}(x) = \begin{cases} log_2 & x + \delta \leq \lfloor x \rfloor + \frac{1}{2} \\ \lceil x \rceil & x + \delta \leq \lfloor x \rfloor + \frac{1}{2} \end{cases}$

With SR, we can perform unbiased quantization of the GEMM operands in the backward pass and ultimately compute unbiased gradient estimates with pure-MXFP4 GEMMs. However, since SR is stochastic, it adds variance to the GEMM output. First, we characterize the variance SR adds to a MXFP4 GEMM:

Theorem 1 Let A and B be two size-b vectors $\in \mathbb{R}^b$, and let \mathcal{Q} perform Algorithm 2. Then, the variance of $\mathcal{Q}(A)^T\mathcal{Q}(B)$ is $\mathcal{O}(b\|A\|_{\infty}\|B\|_{\infty})$

Since the variance of the output is bounded by the largest magnitude element, we can reduce the variance by applying a random orthogonal transform to the operands. In our experiments, we use the **random Hadamard transform (RHT)**, which is *fast to randomize* and runs in *O(n log n)* time. The RHT performs

$$x \leftarrow HSx$$
 $H_n = \frac{1}{2^{n/2}} \begin{bmatrix} H_{n-1} & H_{n-1} \\ H_{n-1} & -H_{n-1} \end{bmatrix}$

and lets us bound the variance of the MXFP4 SR GEMM output:

Theorem 2 The variance of $\mathcal{Q}(HSA)^T\mathcal{Q}(HSB)$ is, with probability $\geq (1 - \epsilon)^2$, $\mathcal{O}(\log(2b/\epsilon)||A||_2||B||_2)$

Hardware Considerations

Directly applying the RHT is inefficient due to how LLMs are trained. When computing $dL/dW = (dl/dy)^T x$, the RHT happens along the batch dimension. In data-parallel setups where data is sharded across devices, this requires expensive communication. Furthermore, while the RHT admits a O(n log n) matrix-vector product, doing so still adds FLOPs to already *compute bound* training.

We solve these problems by applying a blockwise RHT along a small number (~2-4) of MX blocks (Algorithm 3). This makes the RHT *memory bound* on modern accelerators while still achieving good quality due to MX's scaling.

Algorithm 3 MXFP4 linear layer (no bias) backward pass with the random Hadamard transform.

Require: Gradient of output $\frac{dL}{dy} \in \mathbb{R}^{b \times m}$, activations $x \in \mathbb{R}^{b \times n}$, weights $W \in \mathbb{R}^{m \times n}$, block size $g \leq 256, 32|g, g|m, g|n$.

1: $H \leftarrow \text{Hadamard matrix } H_b \in \mathbb{R}^{m \times m}$.

2: Sample random sign vector $S \in \{\pm 1\}^b$.

3: $G' \leftarrow \left(\left(\frac{dL}{dy}\right).\text{view }\left(\frac{bm}{g},g\right)\right) \text{diag}(S)H$

 $4: \ W' \leftarrow H^T \mathrm{diag}(S) \left(W. \mathrm{view} \left(g, \frac{nm}{g} \right) \right) \\ 5: \ GT' \leftarrow \left(\left(\frac{dL}{dy}^T \right) . \mathrm{view} \left(\frac{bm}{g}, g \right) \right) \mathrm{diag}(S) H$

 $6: \ X' \leftarrow H^T exttt{diag}(S) \left(x. exttt{view}\left(rac{bn}{g},g
ight)
ight) \ 7: \ rac{dL}{dx} \leftarrow exttt{MXFP4_GEMM}(G',W')$

8: dL/dW ← MXFP4_GEMM(GT', X')
{Where MXFP4_GEMM forms MX groups along the reduction dimension and uses either Algorithm 1 or 2 to quantize to MXFP4.}
9: if Using Algorithm 2 then

9: **if** Using Algorithm 2 **th**10: $\frac{dL}{dx} \leftarrow \frac{16}{9} \frac{dL}{dx}$ 11: $\frac{dL}{dW} \leftarrow \frac{16}{9} \frac{dL}{dW}$ 12: **end if**13: **return** $\frac{dL}{dx}$, $\frac{dL}{dW}$

Effect of RHT Blocksize

As expected (Theorem 2), increasing the RHT blocksize improves quality. However, increasing the blocksize past a certain point (~256) makes the RHT compute bound, slowing down training.

Table 4: Validation perplexity for training GPT 345M on 33B tokens with various RHT blocksizes. Increasing the RHT block size improves performance by reducing the variance of stochastic rounding.

BW Pass	FP16	INT8 no RHT		•	+ RHT G=128	•	+ RHT G=1024 DENSE	$+ RHT$ G=1024 $\mathcal{O}(n \log n)$
$\overline{\mathrm{E2E}}$ tok/s	46983	55469	67306	64335	64171	63979	61186	62640
BW tok/s	72563	94688	133952	123056	122734	121823	112299	120495

Table 5: Throughput for a FP16 forward pass and specified backward pass of a Llama 2 70B decoder layer. Measured on a NVIDIA A100; see Section 4.2 for more details. Since the A100 can perform INT4 GEMMs 4× faster than FP16 GEMMs, these numbers represent the expected speedup of MXFP4 on supported hardware.